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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,364	07/03/2003	Koji Nii	402691	5401

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EXAMINER	
NGUYEN, LONG T	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 10/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,364	NII, KOJI	
	Examiner	Art Unit	
	Long Nguyen	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *12-17 and 19-21* is/are pending in the application.

4a) Of the above claim(s) *14,15,17 and 21* is/are withdrawn from consideration.

5)☒ Claim(s) *12,13,19 and 20* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 12, 13, 19 and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Kano (USP 5,166,55).

With respect to claims 12 and 13, Figure 2 of the Kano reference discloses a driver, which includes: an input (10); an output (20); a first transistor (26); a first voltage (Vdd); a first internal node (G11); a second transistor (39); a second internal (G14); a second voltage (ground); a third transistor (27); a control circuit (also called as timing circuit, elements 32-33 and all of the transistors in CMOS NOR gate 34 except for the NMOS transistor having its gate connected to input 19 and its drain connected to the output of NOR gate 34); and a fourth transistor (the NMOS transistor inside NOR gate 34, wherein the NMOS transistor having its gate connected to input 19 and its drain connected to the output of NOR gate 34, note see Figure 1.7b of Weste for evidence of the detail of CMOS NOR gate) wherein the second transistor (39) has a driving force higher than a driving force of the third transistor (27, see lines 51-57 of Col. 4 and lines 2-7 of Col. 6). Note that the control circuit (timing circuit) supplying one of the first and second voltages to the second internal node (G14) for a predetermined of time (output waveform of 34), and the timing circuit adjust the predetermined period accordance with the voltage of the output node (base on the feedback from output 20 to the input of inverter 32). Also note that each of the

first to fourth transistors are field effect transistors having respective oxide films (FETs having gate so having gate oxide films). Note for claims 19-20, the timing circuit (elements 32-33 and all of the transistors in CMOS NOR gate 34 except for the NMOS transistor having its gate connected to input 19 and its drain connected to the output of NOR gate 34), the fifth and sixth transistors are the two series PMOS transistors inside of NOR gate 34 (see Weste et al. for evidence of the detail of CMOS NOR gate), and an inverter (32). Note that, for the series connected PMOS transistors inside CMOS NOR gate 34, the fifth transistor is the PMOS having its gate connected to input 19, and the sixth transistor is the PMOS transistor having its gate connected to the output of inverter 32.

Allowable Subject Matter

3. Claim 16 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed on 7/22/05 have been fully considered but they are not persuasive.

Applicant argues that Kano does not disclose or suggest a fourth transistor. However, this argument is not persuasive because, as discussed above, the fourth transistor is the NMOS transistor inside NOR gate 34, wherein the NMOS transistor having its gate connected to the input 19 and its drain connected to the output G14 (see Figure 1.7b of Weste et all for evidence of the detail of CMOS NOR gate).

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directly to Examiner Long Nguyen whose telephone number is (571) 272-1753. The Examiner can normally be reached on Monday to Thursday from 8:00am to 6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached at (571) 272-1740. The fax number for this group is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

LONG NGUYEN
PRIMARY EXAMINER